Memory Module Reliability Qualification

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1.0 Introduction

The purpose of this paper is to describe the various failure mechanisms that could exist in a memory module and the screening processes and profiles that are best for precipitating them. For evaluating memory reliability the following areas of the product shall be evaluated:

1. Solder joint strength limit
2. Solder joint fatigue strength
3. Circuit Board fatigue strength
4. Component failure mechanisms
5. Product susceptibility to moisture related failures

Each of these areas may require unique forms of stimulus and screening profiles to successfully expose any design or process weaknesses.

Our first consideration is the operating conditions of the product. Most memory devices are specified for use between 0ºC and 70ºC. With this in mind, all the screening profiles for functional environmental performance or design/process defect precipitation must be sure to exercise the product at levels which demonstrate adequate margin beyond the specified operating limits.

2.0 References

1. *'Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies'*, IPC-TR-476A,

2. *'Steady State Temperature Humidity Bias Life Test'*, JEDEC Standard JESD22-A101-B,

3. *'Acceptability for Electronic Assemblies'*, IPC-A-610C

4. *'Test Methods Manual'*, IPC-TM-650

5. *'Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments'*, IPC-9701

6. *'Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments'*,IPC-SM-785

7. *'Temperature Cycling'*, JEDEC Standard JESD22-A104-B,

8. *'Environmental Stress Screening Guidelines for Assemblies'*, Institute of Environmental Sciences, 1990

9. Hobbs, G.K., HALT, HASS, *Precipitation and Detection Screens*.

10. Jensen, F. and Petersen, N., *'Burn In'*, John Wiley and Sons, New York, 1982

11. Kececioglu, D., Sun, F.,*'Environmental Stress Screening'*, Prentice Hall, 1995

12. Kececioglu, D., Sun, F., *'Environmental Stress Screening : Its Quantification, Optimization and Management'*, Prentice Hall, 1995

13. Kececioglu, D., *'Reliability Engineering Handbook, Volume 2'*, Prentice Hall, 1991

14. Proceedings of IEEE 1997 Workshop on Accelerated Stress Testing

15. Saari, A.E., Schafer, R.E., VanDenBerg, S.J., *Stress Screening of Electronic Hardware'*, Rome Air Development Center, 1982

16. Schlagheck, J., *Environmental Stress Screening*

17. Tustin, W. and Mercado R., *Random Vibration in Perspective*

18. Engelmaier, W. Apex 2004 Tutorial 02,"*Interconnection Failures and Design Reliability for Plated-Through Holes/Vias (PTHs/PTVs),*

3.0 Solder Joint Reliability Evaluation

For solder joints we have other considerations based on studies of solder joint failure mechanisms and empirical data. In thermal shock screening, the stresses imposed on a solder joint are a result of warpage of the surface mount assembly and the differences in the coefficient of thermal expansion between the materials which comprise the surface mount assembly. During rapid temperature change, the warpages result in tensile and shear stresses on the solder joint. Even assemblies with matched coefficients of thermal expansion will exhibit solder joint failures when subjected to thermal shock. In figure 1 below, a stress/strain chart shows the characteristics of solder joints during thermal cycling. As the solder joints are brought to the highest temperature, the leaded and leadless devices will develop internal stresses and will also exhibit some elastic yielding. Over time, the solder joints will creep to provide stress relaxation. The leaded components also have different stress relief characteristics as the lead, in addition to the solder joint, contribute to the stress relieving process. After the solder joint completely stress relieves and the solder joint is brought to the lowest temperature, the stress and stress relaxation processes occur in the same manner as for the high temperature case described previously. To provide the optimum level of stress relation of the solder joints during the thermal shock screen, a dwell at each temperature extreme must be provided. The solder joint can fully relax in minutes at high temperature and days at very low temperatures. Generally, a dwell time of five to fifteen minutes is prescribed for most screens.

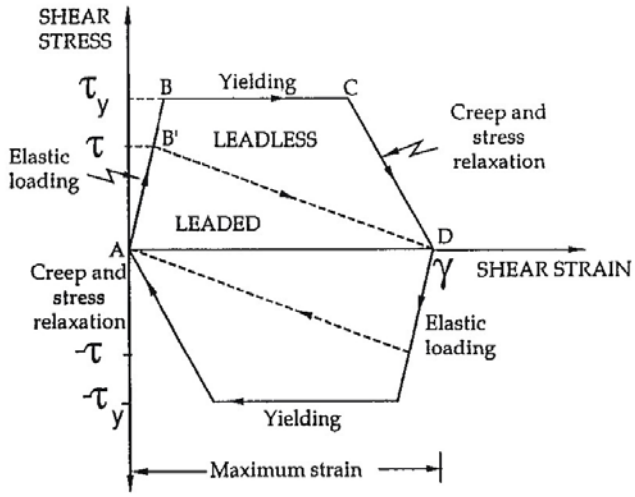

Figure 1 – Stress/Strain diagram for solder joint loading during thermal stress

Another study was performed to determine the optimum temperature range for the temperature cycling screens. The temperature range is the magnitude of the total temperature change from the lowest temperature to the highest temperature. Figure 2 below shows that the number of lifecycle loads was minimized when the temperature range was 120°C.

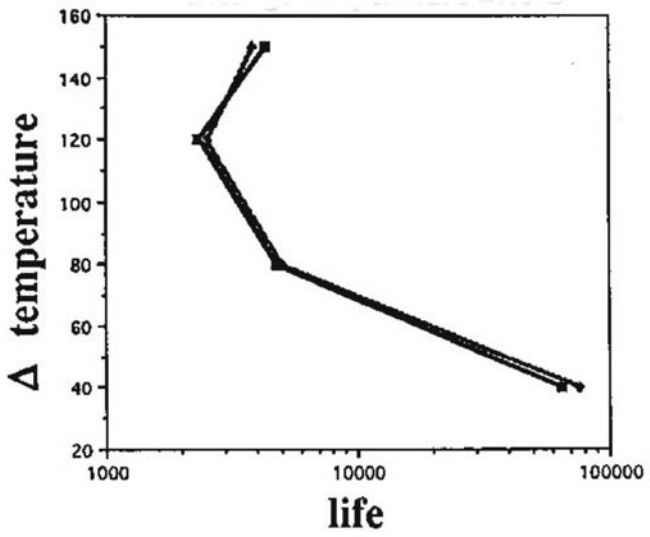

Figure 2 – Solder Joint Lifetime as a function of thermal cycling temperature range

In addition to the temperature range, the temperature rate of change must be determined. Figure 3 below shows a relationship between the temperature rate of change and the number of thermal cycles needed to precipitate a set of seeded defects. Clearly the faster rates of change are more effective at exposing mechanical weaknesses in solder attachments.

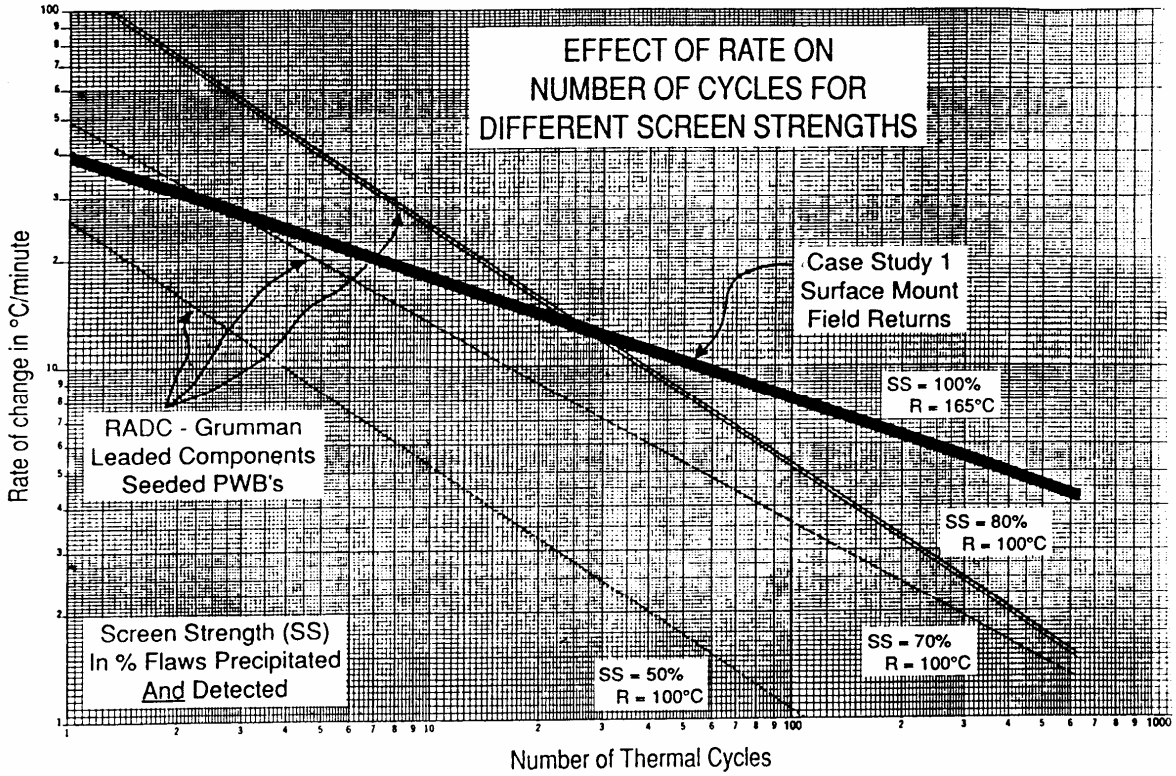

Figure 3 – Number of thermal cycles as a function of rate of temperature change

The previous results are summarized below and also lead us to the establishment of a baseline screen for determining solder joint fatigue strength.

1. Solder joints are best exercised when adequate dwell time is provided to allow for the solder joint to stress relieve. Allow 5 to 15 minutes.
2. The solders joints are best exercised when the temperature range is 120ºC.
3. Rapid temperature changes induce greater levels of stress.
4. The maximum number of cycles is generally accepted to lie between 500 and 1000.

These requirements, along with the product operating specifications, suggest the screening profile for thermal cycling as shown below:

Table 1 - Loaded circuit board screening profile

Parameter	Value or Range
Temperature Range	-10ºC to 110ºC
Temperature Rate of Change	15 ºC/minute to 40 ºC/minute
Soak times	15 minutes at each extreme
Number of Cycles	500 to 1000 (R/O at 168, 336, 668 and 836)

4.0 Circuit Board Reliability Evaluation

Unlike solder attachments, circuit boards have different defect precipitation modes. For circuit boards were we are more interested in plated through hole fatigue strength, innerlayer conductor integrity and laminate integrity. Fortunately, the evaluation of circuit boards do not require the circuit board to be populated and, therefore, reduces the cost of committing material to the reliability program. The primary load driver for stress during a reliability screen for circuit boards arises from the difference in thermal expansion of the circuit board in the X and Y directions verses the Z direction. For standard FR4, the CTE in the X and Y direction is about 15 ppm/°K while the CTE in the Z direction is about 50 ppm/°K. As the circuit board crosses the glass transition temperature (125°C to 170°C), the CTE will increase substantially. At these temperatures, plated through vias can exhibit many failures modes such as:

1. barrel cracks at the center of the PCB at the prepreg layer
2. surface land rotation as a result of Z-axis bulging which can also lead to hole shoulder fracture
3. Inner layer separation at junction of inner foil layer and barrel wall
4. Inner layer separation due to foil fracture

Circuit board structures can be exercised for these types of failure modes during a reliability test through thermal cycling, thermal shock or interconnect stress testing (IST). Since IST relies on specially designed coupons to daisy-chain vias, we will confine our experimentation to thermal cycling or thermal shock as the preferred method to introduce stress for non-coupon based test samples. The profile for a thermal cycling regimen is shown below. Profiles of this type have proven to expose design or process weaknesses to a measurable level in as few as 100 cycles.

Table 2 - Bare circuit board screening profile

Parameter	Value or Range
Temperature Range	Up to -55°C to +160°C
Temperature Rate of Change	Not too important except to reduce test time
Soak times	30 minutes at each extreme
Number of Cycles	100-150

Another form of circuit board failure is caused by the growth of conductive anodic filaments (CAFs). CAFs differ from dendritic growth in that the migrating metal is copper, the filament growth is from anode to cathode and the filament is composed of a metallic salt with the most common anion being chloride. The growth rates of CAFs are controlled by the presence of voltage, humidity and temperature in addition to contamination, process effects, substrate materials, electrode materials and circuit geometry/spacing. Most test cases for CAF formation use temperature, humidity and bias voltage to accelerate the failure mechanism. For bare boards, the applied bias voltage is usually much higher than normal operating voltages and are only limited by the conductor width, conductor spacing and dielectric properties. For memory modules, our desire is to qualify all the materials and processes which were used to produce the module. This requires the module to be populated with the memory devices and,

therefore, prohibits the application of high bias voltages. Table 3 below shows a popular screening profile for accelerating the formation of electro-chemical migration.

Table 3 – Electro-chemical Migration Precipitation Screen

Parameter	Value or Range
Temperature	85°C
Humidity	85%
Number of Hours	500 (R/O at 168 and 336)
Bias Voltage	Bias applied on alternate edge connector pins, VCC and GND are maintained their appropriate voltage levels

5.0 Memory device failure mechanisms and Screening Processes

Memory device failures result from a wide range of causes. Some of the memory device failure causes are:

1. Failures of assembly
2. Failures of packaging
3. Failures of interconnects
4. Failures of the transistors
5. Early failures due to deficiencies in mfg quality
6. Long term failures due to wearout from basic physical or chemical processes
7. Parameter drifts
8. Non destructive latch up (a recoverable failure)

5.1 Assembly failures

The prominent failure due to assembly is failures in die bond attachment.

5.2 Packaging failures

The packages sizes and materials influence the susceptibility package related failures Smaller packages are not as good for strength and moisture protection as larger devices and large differences in CTE between die and package induce shearing and tensile stresses on the die and bond wires. Table 4 below shows the CTE for the various materials used inside memory devices. During thermal cycling, the stress is the greatest at the package corners. A failure of the epoxy packaging can promote moisture absorption. The ingress of moisture can lead to dendritic growth, aluminum track corrosion and popcorn effect.

Table 4 - Expansion coefficients of materials inside memory devices

Material	Thermal Expansion Coefficient
Silicon	2.5×10^{-6}
Copper (Lead Frame)	17×10^{-6}
Die Attach Adhesive	20×10^{-6}
Epoxy (< Glass Transition, 180-225°C)	15×10^{-6}
Epoxy (> Glass Transition, 180-225°C)	40×10^{-6}

5.3 Interconnect Failures

In wire bonding, the gold and aluminum intermetallics are weaker than the original materials and aluminum diffusion into intermetallics cause the Kirkendall voids that can lead to interconnect failure.

5.4 Transistor and die failures

Failures of the silicon die can be caused by many sources. Some of these sources are shown in table 5 below. Some of these failure mechanism are influenced by applied voltage and humidity. A failure mechanism such as electromigration can only occur with an applied bias. Electronmigration can lead to stress voiding which will cause the current density across a track to increase. A failure due to electromigration can occur when the current density approaches 100 amperes per square centimeter.

Table 5 – Die failure mechanisms

Failure Mechanism	Other influences	Result
Dielectric Breakdown and Gate Oxide Defects	Electric field (voltage, dielectric thickness)	Shorts, inactive transistors
Intermetallic Formation	Contamination from package	Open circuits
Poly to metal defect		High resistance
Silicon junction defects	Voltage	Short circuits
Metalization	Composition , doping	Normally open, short
Electromigration	(current. Metal cross section defects)	Open circuits
Ionic contamination	Voltage	Electrical leakage, open circuit , threshold shifts
Charge loss (EPROM's)	Radiation. Repeated switching	Incorrect memory state
Corrosion	Relative humidity. Faulty packaging	Leakage currents. Incorrect memory state. Open circuits
Stress voiding	Mechanical stress	Open circuit. Electromigration

The main source of failures for transistors is dielectric breakdown of the MOS gate dielectrics. The susceptibility of gate oxide failure is directly related to the electric field across the oxide layer and the thickness of the oxide layer. The magnitude of the electric field across gate oxide is at several million volts per cm. Table 6 below shows the life expectancy of a 10nm oxide layer at 150°C for several electric field values. When the oxide layer thickness is reduced by half, the time to failure increases by six orders of magnitude.

Table 6 – Oxide life expectancy for 10nm oxide layer

Electric field value (Mv/cm)	Life expectancy
3.25	11 years
5.0	119 days
6.0	25 days
7.0	2 hours
8.0	54 seconds

The appropriate screening process for memory devices is largely dependent on the expected failure modes. Table 11 on the next page shows several IC failure mechanisms and the best screens for precipitating them. For structural type defects, thermal cycling, thermal shock and random vibration are good choices. For corrosion mechanisms and package seal defects, temperature and humidity as a combined environment is the best choice especially after a precipitation screen such as thermal shock. For electromigration, high temperature (85°C to 150°C) with applied bias is the best choice. The tables below provide suggested screen profiles for each of these failure mechanisms. In most test plans, the products will be subjected to isothermal aging before the precipitation screens to simulate a reasonable use period and to accelerate solder grain growth, intermetallic compound growth and oxidation. The preconditioning screen is generally 24 hours at 100°C.

Table 7 – Structural Defects Precipitation Screen (without vibration)

Parameter	Value or Range
Temperature Range	Up to -55°C to +125°C
Temperature Rate of Change	25°C to 40°C
Soak times	5 minutes at each extreme
Number of Cycles	500 (R/O at 168 and 336)
Bias Voltage	None applied

Table 8 – Structural Defects Precipitation Screen (with vibration)

Parameter	Value or Range
Temperature Range	Up to -55°C to +125°C
Temperature Rate of Change	25°C to 60°C
Soak times	10 minutes at each extreme
Number of Cycles	20
Bias Voltage	None applied
Random Vibration	5 to 15Grms applied during last 5 minutes of soak

Table 9 – Corrosion Defect Precipitation Screen

Parameter	Value or Range
Temperature	85°C
Humidity	85%
Number of Hours	500 (R/O at 168 and 336)
Bias Voltage	Bias applied on alternate edge connector pins, VCC and GND are maintained their appropriate voltage levels

Table 10 – Electromigration Defect Precipitation Screen

Parameter	Value or Range
Temperature	125°C
Number of Hours	500 (R/O at 168 and 336)
Bias Voltage	Device is power and dynamic stimulus applied to exercise internal conductive paths. A less effective but easier approach is to bias the module as in the corrosion defect precipitation screen above.

Table 11 – IC Failure Mechanism and the best screens for precipitation or detection

Screening Test	IC Failure Mechanisms										
	Substrate mounting defects	Bulk silicon defects	Substrate surface defects	Bonding and Wire	Partricle contamination + extraneous material	Seal Defects	Package Defects	External lead defects	Thermal Mismatch	Corrosion	Electrical stability
Internal visual exam	•		•	•	•		•				
External visual exam						•	•	•			
Stabilization bake		•	•	•							•
Thermal Cycling	•		•	•		•	•		•		
Thermal Shock	•		•	•		•	•		•		
Centrifuge	•			•	•		•				
Shock	•			•	•		•				
Vibration	•			•	•		•				
X-Ray	•			•	•	•	•				
Burn-in	•	•	•	•							•
Leakage Tests						•					
Temperature /Humidity						•				•	

6.0 Strength Margin Testing

Strength margin testing closely follows the methodologies of a process called highly accelerated life test (HALT). The purpose of HALT is to expose design weaknesses by iteratively subjecting the product to increasingly higher levels of stress. The two most effective forms of stress are rapid thermal cycling over broad temperature ranges and 3-axis random vibration. Other forms of environmental stress are possible and are largely product dependent.

The byproduct of the HALT is the empirical determination of a set of limits for the product. The limits will include the upper operating limit, the upper destruct limit for temperature and vibration along with the lower operating limit and the lower destruct limit for temperature only. For design, the primary goal of the HALT is to place as much margin between the products specified or guaranteed operating limits and the observed operating limits during the HALT. Studies have consistently shown that products with generous performance margins between the specification and actual performance are inherently more reliable. The determination of the destruct limits are used to ensure that sufficient margin exists between the operating and destruct limits, look for more opportunities for product design/process improvement and to establish a baseline for a production level highly accelerated stress screen (HASS). For some products, the search for the destruct limits may be aborted when the product exhibits survivability well beyond the previously determined operating limits or survivability at the limits of the screening equipment.

The approach for HALT involves the singular and combined application of stresses in the form of temperature and vibration. The stimulus is applied in a step-stress-test approach. During each iteration, the proper functioning of the product is verified before moving to the next higher level of stress. When a product fails to perform while under a specific level of stress, the stress level is reduced to determine if an operating limit has been reached or if the destruct limit has been reached. For memory modules, the “temperature only” stress test can be performed while the module resides in the target computing environment. For “vibration only” stress testing, the module is screened while fastened to the vibration table and is unpowered. After the stress has been suspended, the module is removed from the test chamber and tested in the target computing environment or memory test system with low levels of stress applied. The application of this low level of stress is called a detection screen. The application of combined stresses is performed in the same manner as the “vibration only” scenario in regards to mounting, powering and subsequent testing.

7.0 Analysis of Test Specimens

After the conclusion of each cycle or time milestone in the screen, the test specimens should be visually inspected to determine if the module shows any significant degradation as a result of the screening. For populated modules, a functional test of the memory module is a fast and effective method to assess operation of the memory devices. The functional test, however, may not be effective at detecting structural integrity failures that do not manifest themselves as an electrical short or open. With that in mind, combination of low power visual, electrical test and microsectional analysis provide the best opportunities to observe all product failures. The table below shows the inspection methods that should be used to evaluate product performance at the conclusion of the screening regimen

Memory Product Feature	Examination Method
Solder Joints (surface)	Visual, 30x magnification
Solder Joints (internal)	Cross section across at least 4 joints on two modules; examine at 100x and 200x
CAF growth	Visual, 30x magnification on all modules subjected to temp/humidity
Memory device functionality	Functional Test/System Test
Circuit board lamination	Cross section across at least 2 locations on to modules; examine at 100x and 200x
Circuit board innerlayer integrity	Cross section across at least 2 locations on two modules; examine at 100x and 200x
Circuit board plated through hole integrity	Cross section across at least 2 locations on two modules; examine at 100x and 200x
Cracks on passive devices	Visual, 50x magnification on all modules subjected to thermal cycling, thermal shock or vibration

8.0 Discussion and Conclusions

The need to effectively exercise and precipitate product defects relating to design and processing requires the application of multiple stress environments. The choice of stress environments is determined by the expected failure modes that are usually gained through experience. For new products and technologies for which no field reliability data exists, the most rigorous reliability programs should be conducted. For products that share technology and processes with products for which extensive field data exists may have a subset of the reliability testing that a new product or technology would undergo. A good baseline for a comprehensive reliability program will include the screens shown below.

Loaded circuit board screening profiles:

Screen 1 – Fatigue endurance for solder joints

Parameter	Value or Range
Temperature Range	-10ºC to 110ºC
Temperature Rate of Change	15 ºC/minute to 40 ºC/minute
Soak times	15 minutes at each extreme
Number of Cycles	500 to 1000 (R/O at 168, 336, 668 and 836)
Number of Modules	10

Screen 2 – Screen for memory devices and passives

Parameter	Value or Range
Temperature Range	Up to -55°C to +125°C
Temperature Rate of Change	25°C to 60°C
Soak times	10 minutes at each extreme
Number of Cycles	20
Bias Voltage	None applied
Random Vibration	5 to 15Grms applied during last 5 minutes of soak
Number of Specimens	10

Screen 3 – CAF and dendritic growth susceptibility

Parameter	Value or Range
Temperature	85°C
Humidity	85%
Number of Hours	500 (R/O at 168 and 336)
Bias Voltage	Bias applied on alternate edge connector pins, VCC and GND are maintained their appropriate voltage levels
Number of Modules	10 (use 5 module from screen 1 and 5 modules from screen 2)

Bare circuit board screening profiles:

Screen 4 – Fatigue endurance for bare board structures

Parameter	Value or Range
Temperature Range	-40°C to +160°C
Temperature Rate of Change	5 ºC/minute
Soak times	30 minutes at each extreme
Number of Cycles	100-150
Number of Unpopulated Modules	10